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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/081,740	02/22/2002	Yvon Bahout	00RO35454405	9492

27975 7590 12/23/2004

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EXAMINER	
BRAGDON, REGINALD GLENWOOD	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/081,740	BAHOUT, YVON	
	Examiner	Art Unit	
	Reginald G. Bragdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 7-15, 17-19, and 25-28 are rejected under 35 U.S.C. 102(b) as being anticipated by "Using Microprocessors and Microcomputers: The 6800 Family" (Joseph D. Greenfield and William C. Wray, hereinafter Greenfield et al.).

As per claim 7, Greenfield et al. teaches the Motorola microprocessor 6800 instruction set, which includes the JUMP instruction, which can be specified in one of two modes, including the Jump Extended mode. See page 116 (in the paragraph above 6-3.2) and figure 6-1(b). As can be seen from figure 6-1(b), the program counter PC ("incremental address counter"; see page 48, section 3-7, for a description of the PC) is loaded with an address value, n, which must be decoded (see page 48, section 3-7, for a description of the instruction decoder, and pages 50-51 for a description of the hardware execution of a simple program) to determine that a JUMP instruction is being executed ("detecting an address jump signal"). Since a JUMP Extended instruction has been decoded, the 6800 system know that the PC must be incremented (to the values n+1 and n+2) in order to read the high and low address bytes of the "JUMP to" address ("reading a content of the memory at the incremented address"). See figure 6-1(b). The high and low address bytes are transferred from the memory to the PC ("transferring the content read

at the incremented address to the incremental address counter"). See page 115, first paragraph of section 6-3.1. The next instruction is read at address value K ("reading the content of the memory at the address contained in the incremental address counter"). See figure 6-1(b) and page 115, first paragraph of section 6-3.1.

As per claim 8, Greenfield et al. teaches that instructions, such as the JUMP instruction, must be decoded. See page 48, section 3-7, "The instruction decoder".

As per claim 9, Greenfield et al., as shown in figure 6-1(b), the program counter is incremented by 1 to read the high order byte of the jump to address.

As per claim 10, Greenfield et al. teaches that the PC is loaded with the address of the next instruction. See figure 6-1(b) and page 116 (in the paragraph above 6-3.2).

As per claim 11, with reference to figure 6-1(b), Greenfield et al. teaches a JUMP instruction, the data buffer shown in figure 8-3 on page 181 represents an "input register" ("providing an instruction code and memory address code to an input register"), where the data buffer receives data (including address values, instructions, and actual data values) from the memory. The JUMP address value (K in figure 6-1(b)) is loaded into the PC ("providing the memory address code to an incremental address counter having an input connected to the input register and an output connected to the memory"), where the PC is connected to the data buffer and address output buffers ("output connected to the memory") over a 8-bit internal bus. See figure 8-3 and page 179, section 8-5. The value of the instruction at K is read ("reading the memory at the memory address code indicated by the incremental address counter"). See figure 6-1(b) and pages 115-116. The contents of the instruction read at K can be read from RAM, which has 3-state output buffers ("output registers"). See figure 8-8 on page 193.

Greenfield et al. further teaches a JUMP instruction, which can be specified in one of two modes, including the Jump Extended mode. See page 116 (in the paragraph above 6-3.2) and figure 6-1(b). As can be seen from figure 6-1(b), the program counter PC ("incremental address counter"; see page 48, section 3-7, for a description of the PC) is loaded with an address value, n, which must be decoded (see page 48, section 3-7, for a description of the instruction decoder, and pages 50-51 for a description of the hardware execution of a simple program) to determine that a JUMP instruction is being executed ("detecting an address jump instruction code using an address jump detection circuit having an input connected to the input register and an output connected to the incremental address counter"). Since a JUMP Extended instruction has been decoded, the 6800 system know that the PC must be incremented (to the values n+1 and n+2; "providing an increment signal from the address jump detection circuit to the incremental address counter based upon the detected jump address instruction code") in order to read the high and low address bytes of the "JUMP to" address. See figure 6-1(b). The high and low address bytes are transferred from the memory to the PC ("transferring the content read at the incremented address to the incremental address counter"). See page 115, first paragraph of section 6-3.1. The next instruction is read at address value K. See figure 6-1(b) and page 115, first paragraph of section 6-3.1.

As per claim 12, Greenfield et al. teaches that the PC is loaded with the address of the next instruction. See figure 6-1(b) and page 116 (in the paragraph above 6-3.2).

As per claim 13, Greenfield et al., as shown in figure 6-1(b), the program counter is incremented by 1 to read the high order byte of the jump to address.

As per claim 14, Greenfield et al. teaches that instructions, such as the JUMP instruction, must be decoded. See page 48, section 3-7, "The instruction decoder".

As per claim 15, Greenfield et al. teaches 3-state switching/selection (section 8-4.3, first paragraph; "transfer circuit") connected between the PC ("incremental address counter") and the output buffers ("output register") of the RAM.

As per claim 17, with reference to figure 6-1(b), Greenfield et al. teaches a JUMP instruction, the data buffer shown in figure 8-3 on page 181 represents an "input register", where the data buffer receives data (including address values, instructions, and actual data values) from the memory. The JUMP address value (K in figure 6-1(b)) is loaded into the PC ("an incremental address counter"), where the PC is connected to the data buffer ("input connected to said input register") and address output buffers ("output connected to the memory") over a 8-bit internal bus. See figure 8-3 and page 179, section 8-5. The value of the instruction at K is read. See figure 6-1(b) and pages 115-116. The contents of the instruction read at K can be read from RAM, which has 3-state output buffers ("output registers") connected to the memory matrix. See figure 8-8 on page 193.

Greenfield et al. further teaches a JUMP instruction which must be decoded (see page 48, section 3-7, for a description of the instruction decoder, and pages 50-51 for a description of the hardware execution of a simple program) to determine that a JUMP instruction is being executed ("address jump detection circuit"), where the instruction decoder is coupled to the data buffers. Since a JUMP Extended instruction has been decoded, the 6800 system know that the PC must be incremented (to the values n+1 and n+2; "address jump detection circuit…and an output connected to said incremental address counter") in order to read the high and low address bytes

of the "JUMP to" address. See figure 6-1(b). Greenfield et al. teaches 3-state switching/selection (section 8-4.3, first paragraph; "transfer circuit") connected between the PC ("incremental address counter") and the output buffers ("output register") of the RAM.

As per claim 18, Greenfield et al. teaches that the PC is loaded with the address of the next instruction. See figure 6-1(b) and page 116 (in the paragraph above 6-3.2).

As per claim 19, Greenfield et al. teaches that instructions, such as the JUMP instruction, must be decoded. See page 48, section 3-7, "The instruction decoder".

As per claim 25, the claim is rejected for the reasons set forth for claim 17, above, noting that the microprocessor is the 6800 microprocessor, including an ALU.

As per claim 26, from figure 6-1(b), it can be seen that the values are read sequentially from memory.

As per claim 27, Greenfield et al. teaches that the PC is loaded with the address of the next instruction. See figure 6-1(b) and page 116 (in the paragraph above 6-3.2).

As per claim 28, Greenfield et al. teaches that instructions, such as the JUMP instruction, must be decoded. See page 48, section 3-7, "The instruction decoder".

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 16, 20-24, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greenfield et al. in view of Nakagawa et al. (5,651,123).

As per claim 21, the claim is taught for the reasons set forth for claim 17, above, except as noted below.

As per claims 16, 20, 21, and 29, Greenfield et al. teaches 8-bit parallel 3-state switching/selection transfer logic for bi-directional transfer over the data bus ("logic gate"). See page 175, section 8-4.3, first paragraph. Furthermore, Greenfield et al. teaches selectively either incrementing a PC or using an address read from memory based on a JUMP instruction, as detailed above for claims 7, 11, 17, 21, and 25. However, Greenfield et al. does not teach a multiplexer circuit connected to the 3-state logic and the PC for selectively providing either an increment signal or an address read from memory based on a JUMP instruction. Nakagawa et al. teaches, with reference to figure 1, a selector 304 ("multiplexer") connected to a program counter, where the selector 304 selects either an incrementer 302 or jump address 44 based on a select signal from an instruction decoder 34. See column 1, lines 43-55. It would have been obvious to one of ordinary skill in the art to have modified Greenfield et al. to include a selector (multiplexer) to select between incrementing the PC or placing a JUMP address read from memory in the PC based on a decoded JUMP instruction signal, as taught by Nakagawa et al., because a 2-input/1 output multiplexer is a simple, readily available component for selecting between two elements.

Response to Arguments

5. Applicant's arguments filed 09 November 2004 have been fully considered but they are not persuasive.

Applicant argues that the claimed invention "sends to the memory not a complete message, but rather an instruction code, i.e. without an address" (page 12 of the response). However, this is not a feature of the claims. The independent claims do not specify that an address is not sent with the instruction code (or alternately, that only the instruction code is sent). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(571) 273-4204**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (571) 272-4204. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (571) 272-4210.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
December 20, 2004